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Robust admittance shaping approach to grid current harmonic attenuation and resonance damping

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***Abstract*—This paper presents a novel grid current control of a grid connected Voltage Source Converter (VSC) with an LCL filter. The proposed control method uses an $\mathcal{H}_\infty$ synthesis method to shape the input admittance of the converter, to track a given current reference and/or to limit the controller actuation at different frequency ranges. The converter admittance is shaped, both in magnitude and phase, following a model reference defined by the designer in the frequency domain. By specifying a low admittance magnitude reference, the optimization algorithm will obtain a controller that actively damp the filter resonance and attenuate/reject the grid voltage oscillations, either in a wide frequency range or concentrated at the main harmonic frequencies. Additionally, the proposed controller design methodology takes advantage of its admittance phase shaping capability to improve the system robustness in front of grid uncertainties and minimizing converter impact over grid stability due to its possitive-real nature. The synthesized controller only measures the grid current and voltage to achieve the aforementioned results, reducing the number of sensors (and their associated cost) required for its implementation. Experimental results illustrate the correct behaviour of the closed-loop system with the designed controller in time and frequency domain.**

I. Introduction

This work presents a new grid current controller structure for a Voltage Source Converter (VSC) connected to the grid through an LCL filter. This topology is very common in renewable energy source based power plants, as it has superior output performance.

However, the resonant behaviour of the LCL filter presents some drawbacks for its effective and stable current control from the point of view of power quality, system robustness and impact of the system on PCC stability.

From the power quality point of view, system resonances -in the grid or the filter- may lead to oscillations, and even to instabilities of the controlled grid current [1], [2]. Many papers have focused on the design of resonance dampers that improve the overall current dynamics. They can be classified into active [2]–[9] and passive [10]–[14] damping techniques. A related issue is the effect of grid voltage harmonics and inter-harmonics in the control loop. The most usual approach is to design the current controllers with harmonic rejection capabilities, mainly by using PR (proportional + resonant) controllers tuned at the most common harmonics in order to reject them [15]–[17]. However, the harmonic rejection performance depends on different factors, such as the model uncertainties, the discretization process and the presence of computational delays in the system [18]. Additionally, the use of high feedback-gain controllers may lead to poor stability margins [19], and its stable operation becomes more difficult as the harmonics to be rejected approach to the filter resonance frequency [20], [21].

From the robustness point of view, it is known that the stability of the control loop of the LCL-filtered grid-connected VSC may be compromised by the uncertainty in the grid output impedance, which may lead to the uncontrolled displacement of resonances inside the control bandwidth. Several approaches to robust control have been explored in literature [22], [23], being achieved at the cost of a conservative performance -control bandwidth reduction- to cope with the uncertainty.

Finally, the growing penetration of power electronic systems in the grid is increasing the concerns related to the potential negative effect of its connection on the power system stability. This problem is known to be related with the constant-power nature of this converters. Although the problem is still under discussion in its more general formulation [24], it is accepted that, when studied arround an operation point, converter input addmitance plays an important role.

This paper deals with the aforementioned problems from an input-admittance shaping point of view. This is possible using the new capabilities of the algorithm presented by authors in [25]. This recent method allows shaping the input admittance transfer function of a VSC, in both magnitude and phase, while maintaining the tracking performance at selected frequencies and optimizing the needed controller actuation.

Admittance shaping techniques open the door to face the robustness problem by trying to comply with certain input admittance conditions derived in the Middlebrook's stability criterion [12], [26]–[29]. This new point of view decreases the deterioration of the closed-loop performance usually induced by traditional robust control approaches in the pressence of big grid uncertainty. If the shaped admittance, additionally, is low, the converter will present a good attenuation of the

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grid voltage (inter) harmonic effect on the controlled current. That condition, over the frequencies corresponding to LCL-filter ressonance, also implies a good damping of it. The tight control of the converter input admitance, allows to minimize the impact of the converter on power system stability.

Satisfaction of previous objectives implies the shaping of different closed-loop functions in different frequency bands: current reference tracking implies the shaping of the complementary sensitivity function arround the fundamental frequency, harmonic response optimization implies the minimization of closed-loop input admittance module over the control bandwidth and positive-real input admittance is obtained by tihgtly controlling admittance phase. The complexity of the objectives makes the problem hard to approach from classical control strategies that, in the reported approaches, offer limitations in their capabilities and scope and, also, imply non-trivial design iterations [30]–[35].

The main contribution of this work is the proposal of a design and synthesis procedure able to deal with those objectives in a systematic and guaranteed way, that results intuitive for the designer. Latter features are inherited from the underlying convex $\mathcal{H}_\infty$ optimization-based synthesis algorithm. This paper is an extension of the research presented in [36], including the posibility of using higher-order admitance-model shaping capabilities to better improve harmonic response while keeping good control of input admittance.

The text is structured as follows: Section II presents the system modelling, its stability analysis and the proposed control objective. Section III explains the proposed admittance shaping method; it gives some guidelines for the design parameters tuning, presents the different control trade-offs, enumerates the limitations of the design methodology and gives some information of the controller synthesis. Section IV applies the proposed methodology to achieve two low admittance designs: one following a broad-band resistive model and another with a higher admittance minimization at selected low order harmonics. Section V presents the achieved experimental results of both proposed designs in both time and frequency domains. It demonstrates the good resonance damping, the attenuation/rejection of grid voltage (inter) harmonics effect in the controlled current and the robustness of the proposed method towards weak grids. The paper concludes with Section VI.

II. System Modelling, its Stability Analysis and the Control Objective

A. System modelling

Fig. 1 shows a single-phase equivalent of the considered system: a grid current i control of a grid-connected VSC with an LCL filter. This single-phase system is considered for both modelling and controller design procedures. The obtained controller can be easily translated and implemented in a three-phase system using $\alpha\beta$ stationary reference frame transformations [37] for its input and output signals.

Neglecting for now the time delay and PWM effects on the VSC output voltage (i.e., a $u^* = u$ is considered in Fig. 1), the open-loop grid current can be expressed in Laplace domain

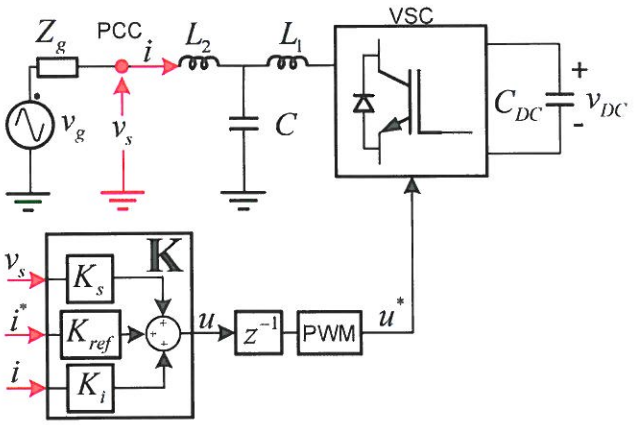

Fig. 1. Simplified single phase equivalent of the considered VSC-based system.

as follows:

$$I(s) = G(s)U(s) + G_d(s)V_s(s), \tag{1}$$

where $I(s)$, $U(s)$ and $V_s(s)$ are the grid current, controller output voltage and point of common coupling (PCC) voltage, respectively, and $G(s)$ and $G_d(s)$ are the open-loop command-to-output and admittance transfer functions;

$$G(s) = -\frac{1}{sC(R_1 + sL_1)(R_2 + sL_2) + R_f + sL_f} \tag{2}$$

$$G_d(s) = \frac{sC(R_1 + sL_1) + 1}{sC(R_1 + sL_1)(R_2 + sL_2) + R_f + sL_f} \tag{3}$$

where C, L_1 and L_2 are the filter capacitor and the converter-side and grid-side filter inductance values, respectively, and R_1 and R_2 are their respective parasitic resistances, with $L_f = L_1 + L_2$ and $R_f = R_1 + R_2$. Both functions have a resonant frequency ($\omega_{res} = \sqrt{L_f/(L_1 L_2 C)}$), where their respective magnitudes increase, that represents a risk factor for the system stability.

The grid current controller $\mathbf{K}$ shown in Fig. 1 is implemented in the discrete-time z domain. The open-loop grid current dynamic shown in (1) is therefore affected by a discrete and delayed controller output u and the grid voltage v_s, which is still a continuous disturbance to it. To model this more realistic hybrid continuous/discrete scenario, the open-loop command-to-output transfer function $G(s)$ defined in (2) is modified as follows. First, it is discretized to $G_{ZOH}(z)$ using a ZOH; this step represents a close approximation of the PWM block effect in the actuation voltage u. Then, the computational delay is modelled by adding a z^{-1} term to $G_{ZOH}(z)$, resulting in $G_z(z) = z^{-1}G_{ZOH}(z)$. Finally, a continuous approximation $G(s)$ of $G_z(z)$ is obtained by using the bilinear transformation, making a pre-warping to accurately preserve the LCL resonance frequency. $G_d(s)$ is modelled following (3), as the PCC voltage is, as mentioned, a continuous disturbance to the process.

A three degrees-of-freedom (DOF) controller $\mathbf{K}$ is con-

sidered in this paper[1]. Its inputs are the PCC voltage v_s, the grid current i and the reference current i^*. The only measurements necessary for the controller implementation are, then, the grid currents and voltages[2]. Dividing the controller matrix in columns $\mathbf{K}(s) = [K_s(s) \quad K_{ref}(s) \quad K_i(s)]$ results in the closed-loop current dynamics shown below;

$$I|_{Z_g(s)=0} = \underbrace{\frac{GK_{ref}}{1-GK_i}}_{T(s)} I^* + \underbrace{\frac{G_d+GK_s}{1-GK_i}}_{Y(s)} V_s, \qquad (4)$$

where $T(s)$ and $Y(s)$ are the closed-loop tracking and admittance transfer functions for an ideal grid (i.e., grid impedance $Z_g(s) = 0$). A system that behaves like a low admittance in a wide range will attenuate the impact of grid voltage harmonic/inter-harmonics on the controlled current and damp the LCL filter open-loop resonance by reducing its magnitude.

The closed-loop controller actuation dynamic can be expressed as[3]:

$$U|_{Z_g(s)=0} = \underbrace{\frac{K_s+K_iG_d}{1-GK_i}}_{F_{v_s\to u}(s)} V_s + \underbrace{\frac{K_{ref}}{1-GK_i}}_{F_{i^*\to u}(s)} I^* \qquad (5)$$

Higher $|F_{v_s\to u}|$ and $|F_{i^*\to u}|$ will result in higher actuation u levels for changes in the PCC voltage v_s (e.g. grid voltage dips, harmonics, etc.) or the current reference i^*, that may leed to overmodulation behaviour.

B. Stability analysis of the system

Assuming linearity, the stability of a current-controlled VSC connected to an ideal grid only depends on the analysis of the stand-alone loop function $L(s) = -GK_i$ in (4) and (5). The maximum magnitude peak $M_s = \|S\|_\infty$ of the sensitivity transfer function $S = (1+L(s))^{-1}$ is a good inverse indicator of the system stand-alone stability robustness, as the minimum distance (d_{min}) from the polar plot of $L(s)$ to the point $-1+j0$ is $d_{min} := M_s^{-1}$. A smaller M_s value means, then, larger stability margins. An usual good design bound is $M_s \leq 2$ (6 dB) [38]. That will assure a gain margin $GM > 6$ dB and a phase margin $PM > 30^o$.

When the system is connected to a grid with a non-negligible equivalent series grid impedance Z_g, the controlled-current i follows the following dynamic:

$$I|_{Z_g(s)\neq 0} = \underbrace{\frac{T}{1+Z_gY}}_{T'(s)} I^* + \underbrace{\frac{Y}{1+Z_gY}}_{Y'(s)} V_g, \qquad (6)$$

where V_g is the ideal (stiff) grid voltage and $Y'(s)$ and $T'(s)$ are the modified closed-loop admittance and tracking transfer functions, respectively.

From (6), it can be seen that the system stability depends on the VSC stand-alone stability (derived from $L(s) = -GK_i$ analysis in (4) and (5)), but also on the new impedances loop function $L'(s) = Z_gY$. That is, provided that the VSC-based system is stand-alone stable, the stability of its connection with the grid relies on the relationship between Z_g and Y [12], [26]. Several criteria have been proposed in the literature to impose certain VSC admittance Y conditions to achieve stability for a given grid impedance Z_g uncertainty [12], [31], [39]. One particularly interesting approach is to take advantage of the Strictly Positive Realness of function Z_g [40]: if the grid impedance Z_g and the rendered Y are positive real the system is stable regardless of the functions respective magnitudes. That is, a resistive, or at least passive, behaviour of the controlled VSC will improve its stability robustness with a wide range of grid impedances [34], [41], [42].

C. Objectives

The objective of this work is to obtain designs with the next characteristic; a low admittance value to reject/attenuate voltage (inter) harmonics and damp the LCL filter resonance, and a passive behaviour in the broadest bandwidth possible to improve the system robustness towards grid uncertainties and to minimize converter impact into power system stability. In addition, the proposed design should track a given current reference i^* with enough robust stability margins, and limit the controller actuation to avoid potential saturation problems and optimize the energy required.

Due to its importance on a power system scenario with an increasing number of converters connected to it, those later objectives have been previously studied in the literature, although the number of references is not big due to its novelty. Most approaches are based on the modification of classic controllers to modify the converter admittance on certain frequencies. The inherent complexity of the objective limits the possibilities and scope of these approaches, due to the necessity of handling, simultaneously, different objectives affecting to closed-loop function in modulus and phase [30]–[35].

The present proposal uses the capabilities of modern $\mathcal{H}_\infty$ techniques to face those objectives in a unified framework, offering a easy interfaces for the designer and guaranteeing the synthesis of a (sub)optimal controller.

III. Model-Reference Approach to Admittance Shaping

The desired controller is obtained following a model reference $\mathcal{H}_\infty$ design approach [38], [43]–[45]. The application of this method to the admittance shaping of VSC was previously presented in [25]. This section summarizes the design methodology of this new technique.

A. Theoretical background

The keystone of the $\mathcal{H}_\infty$ control paradigm is the definition of the inner structure of the generalized plant $\mathbf{P}$. Fig. 2 shows, in red, the structure of this plant for the presented admittance shaping method. It is formed by the open-loop current dynamic in (1), shown in orange, and some design parameters, shown in purple, only added for the controller synthesis process. $\mathbf{P}$

[1]For notation compactness, the Laplace variable 's' is omitted when its presence is obvious, attending to the context

[2]Note that the grid PCC voltage is usually available at no extra sensor cost as the grid synchronisation algorithms use it.

[3]The notation $\mathbf{F_{u\to y}}$ is used to define a transfer function/matrix with inputs $\boldsymbol{u}$ and outputs $\boldsymbol{y}$.

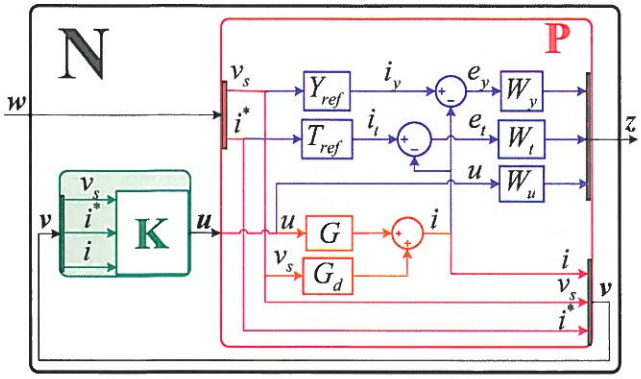

Fig. 2. $\mathcal{H}_\infty$ model-reference approach to admittance shaping control. The generalized plant $\mathbf{P}(s)$ is represented in red. Inside of it, the open loop command-to-output $G(s)$ and admittance $G_d(s)$ transfer functions (in orange), and a set of elements (in purple), added for the $\mathcal{H}_\infty$ controller synthesis, which serve as the main design parameters. Finally, the future synthesized controller $\mathbf{K}$ is represented in green.

has the next inputs and outputs: input vector $\boldsymbol{w}$, formed by the disturbances to the closed-loop system v_s and i^* (see (4) and (5)); input $\boldsymbol{u}$ and output vector $\boldsymbol{v}$, which are equal to the controller $\mathbf{K}$ output (u) and inputs (v_s, i^* and i), respectively; and the output vector $\boldsymbol{z}$, which is formed by the signals to be minimized in the design. Once the designer defines the plant $\mathbf{P}$, the $\mathcal{H}_\infty$ synthesis process will compute the controller $\mathbf{K}$ with inputs $\boldsymbol{v}$ and outputs $\boldsymbol{u}$ that minimises the ∞-norm[4] of the closed-loop generalized transfer function $\mathbf{N}(\mathbf{P},\mathbf{K})$;

$$\min_{\mathbf{K}} ||\mathbf{N}(\mathbf{P},\mathbf{K})||_\infty \leq \gamma \tag{7}$$

where γ is usually a sub-optimal value.

The output vector $\boldsymbol{z}$ and the design parameters are defined as follows. In Fig. 2, $Y_{ref}(j\omega)$ represents the desired behaviour in the frequency domain of the closed-loop admittance $Y(j\omega)$, as so does $T_{ref}(j\omega)$ for the desired tracking transfer function $T(j\omega)$. The obtained controller should fulfil either $T(j\omega) \approx T_{ref}(j\omega)$ or $Y(j\omega) \approx Y_{ref}(j\omega)$ at a given frequency by minimizing the tracking shaping e_t or admittance shaping e_y error signals, respectively. Which one is fulfilled depends on the magnitude of the tracking ($|W_t(j\omega)|$) and admittance ($|W_y(j\omega)|$) frequency weights. The actuation signal (i.e., control effort) u defined in (5) needs also to be minimized to avoid controller saturation problems. To that end, a third weight $W_u(j\omega)$ is added to limit its value at the desired frequencies. The outputs of these three weights will form the minimization vector $\boldsymbol{z}$.

Summing up, $\mathbf{P}$ has the next structure;

$$\begin{bmatrix} \boldsymbol{z} \\ \boldsymbol{v} \end{bmatrix} = \mathbf{P} \begin{bmatrix} \boldsymbol{w} \\ \boldsymbol{u} \end{bmatrix}, \tag{8}$$

[4]The ∞-norm of a transfer matrix $\mathbf{N}$ is defined as the square root of the energy (2-norm) of its output vector $\boldsymbol{z}$ with respect to the worst-case direction and frequency of its unit input vector $\boldsymbol{w}$: $||\mathbf{N}||_\infty = \max_{\boldsymbol{w}\neq 0}\left(\frac{||\boldsymbol{z}||_2}{||\boldsymbol{w}||_2}\right)$. The energy of a signal x is defined as $E_x = ||x||_2^2 = \int_{-\infty}^{\infty} |x(t)|^2 dt$.

where;

$$\boldsymbol{z} = \begin{bmatrix} W_t \cdot e_t \\ W_y \cdot e_y \\ W_u \cdot u \end{bmatrix} \quad \boldsymbol{v} = \begin{bmatrix} v_s \\ i^* \\ i \end{bmatrix} \quad \boldsymbol{w} = \begin{bmatrix} v_s \\ i^* \end{bmatrix} \quad \boldsymbol{u} = u \tag{9}$$

$\|\mathbf{N}\|_\infty$ in (7) can be computed using a lower fractional transformation (LFT) as;

$$\|\mathbf{N}\|_\infty = \left\| \begin{matrix} W_t \boldsymbol{F}_t \\ W_y \boldsymbol{F}_y \\ W_u \boldsymbol{F}_u \end{matrix} \right\|_\infty \tag{10}$$

where;

$$\boldsymbol{F}_y = \boldsymbol{F}_{\boldsymbol{w}\to e_y} = \begin{bmatrix} Y_{ref} - Y & -T \end{bmatrix} \tag{11}$$

$$\boldsymbol{F}_t = \boldsymbol{F}_{\boldsymbol{w}\to e_t} = \begin{bmatrix} -Y & T_{ref} - T \end{bmatrix} \tag{12}$$

$$\boldsymbol{F}_u = \boldsymbol{F}_{\boldsymbol{w}\to u} = \begin{bmatrix} F_{v_s\to u} & F_{i^*\to u} \end{bmatrix} \tag{13}$$

with Y and T defined in (4) and $F_{v_s\to u}$ and $F_{i^*\to u}$ defined in (5).

B. Design parameters selection

It is clear that a $T_{ref} = 1$ is desired to obtain a good current tracking (i.e., $i = i^*$). The admittance profile Y_{ref} is, on the other hand, more dependent of the control objectives. Section IV explores two possible Y_{ref} values to achieve this work objectives. More examples can be found in [25].

The selection criterion of the weights is deduced next. The minimization inequality shown in (7) can be expressed as a stacked problem with three single specifications to fulfil:

$$\bar{\sigma}\left(\boldsymbol{F}_y\right)(j\omega) \leq \frac{\gamma}{|W_y(j\omega)|} \tag{14}$$

$$\bar{\sigma}\left(\boldsymbol{F}_t\right)(j\omega) \leq \frac{\gamma}{|W_t(j\omega)|} \tag{15}$$

$$\bar{\sigma}\left(\boldsymbol{F}_u\right)(j\omega) \leq \frac{\gamma}{|W_u(j\omega)|} \tag{16}$$

where $\bar{\sigma}\left(\boldsymbol{F}_x\right)$ is the maximum singular value of the function $\boldsymbol{F}_x$, that is, its maximum gain value for variations of $\boldsymbol{w}$ direction and frequency [38]:

$$\frac{\|\boldsymbol{F}_x \boldsymbol{w}\|_2}{\|\boldsymbol{w}\|_2} \leq \bar{\sigma}\left(\boldsymbol{F}_x\right), \ \forall\omega \ and \ \|\boldsymbol{w}\|_2 \neq 0 \tag{17}$$

Different conclusions can be derived from inequalities (14), (15) and (16):

1) W_y definition: Attending to the condition given by inequality (14) and $\boldsymbol{F}_y$ definition in (11), it is deduced that a large admittance weight magnitude ($|W_y|$) *should* minimize $\bar{\sigma}\left(\boldsymbol{F}_y\right)$ and, then, the magnitude of both admittance shaping error ($|Y_{ref} - Y|$) and tracking transfer function ($|T|$). That is, high values of the admittance weight *should* result in $Y(s) \to Y_{ref}(s)$, both in magnitude and phase, and $T(s) \to 0$.

2) W_t definition: In the same way, from (15) and (12), a large tracking weight magnitude ($|W_t|$) *should* minimize both tracking shaping error ($|T_{ref} - T|$) and admittance transfer function ($|Y|$) magnitudes, achieving a $T(s) \to T_{ref}(s)$ and $Y(s) \to 0$.

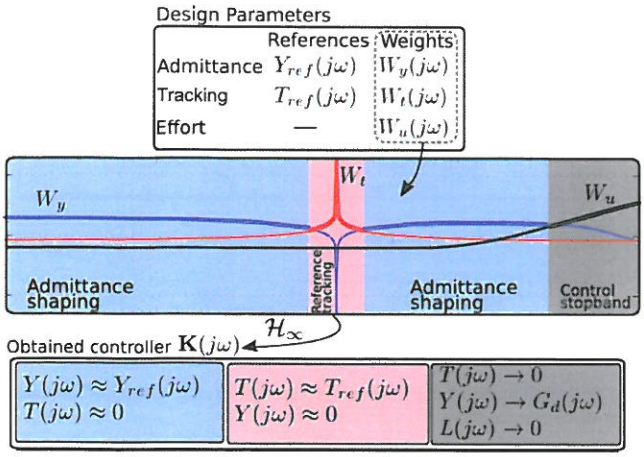

Fig. 3. Weight selection example and the resulting separation of the controller $\mathbf{K}(s)$ objectives in frequency zones.

3) W_u definition: Finally, from (16) and (13), a large control effort weight magnitude ($|W_u|$) *should* result in a minimized $\bar{\sigma}(\boldsymbol{F}_{w\to u})$, and then in a reduced controller actuation u in (5). In other words, a controller $\mathbf{K} = [K_s \quad K_{ref} \quad K_i]$ that tends to zero *should* be expected at frequencies with a large $|W_u|$ definition, resulting in a $T(s) \to 0$ and a $Y(s) \to G_d(s)$ in (4). Additionally, a large $|W_u|$ *should* make the stand-alone loop function $L(s) = -GK_i \to 0$, so increasing $|W_u|$ is the best way to limit the controller bandwidth.

The emphasis in the word *should* in the conclusions above comes from the importance of the obtained γ (defined in (7)) in inequalities (14), (15) and (16). This term acts as an indicator of how *difficult* it is for the $\mathcal{H}_\infty$ synthesis algorithm to obtain a controller that fulfils the design conditions imposed by the information contained in $\mathbf{P}$. In other words, large γ values usually result in a poor minimization of either e_y, e_t or u. Typically, the synthesis is considered successful for $\gamma \leq 1$.

Two main factors may induce a large γ. The first one comes from the interaction between design specifications. Normally, it is not possible to minimize at the same frequencies the tracking error (e_t), the admittance shaping error (e_y) and the control effort (u). To solve this, the design weights must be defined in a complementary manner. That is, if a good admittance shaping is desired, a large $|W_y|$ and a small $|W_t|$ and $|W_u|$ have to be defined; minimization of the tracking error and the control actuation follow an equivalent design guideline. The design limitations induced by the discrete nature of the implemented controller are the second risk factor of a large γ value. These limitations are explained in Section III-D.

Fig. 3 summarizes the expected results of a controller ($\mathbf{K}$) obtained from a given set of model references and complementary design weights. The chosen weights will divide the spectrum in three different frequency zones, each of which is characterized by some controller objective.

C. Design trade-offs

The designer has to deal with two main control trade-offs: good admittance shaping versus good reference tracking capabilities and good controller performance[5] versus energy optimization.

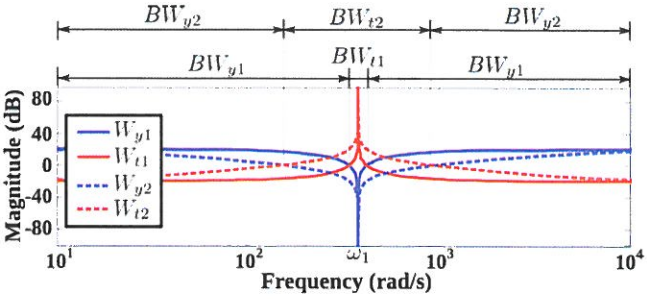

Fig. 4. Admittance versus tracking shaping trade-off example: proposed weights selection for the two considered designs.

The admittance versus tracking trade-off is first illustrated by means of two designs, identified by subscripts 1 and 2 in Figs. 4-6. The selected admittance (W_y) and tracking (W_t) weight magnitudes for these designs are shown in Fig. 4, being the control effort (W_u) equal to zero to simplify the analysis. From this selection, a good admittance and tracking shaping should be expected inside BW_y and BW_t frequency ranges, respectively, with a greater tracking error (e_t) minimization at frequency ω_1 due to the bigger $|W_t|$ at this frequency. The expected admittance shaping results are confirmed in Fig. 5, where the first design admittance (Y_1) follows the given admittance reference (Y_{ref}) in a wider band than the second design (Y_2). However, this wider admittance shaping range comes at the expense of a narrower tracking shaping range, as it is demonstrated in Fig. 6. In it, the tracking function (T) of both designs are equal to the given unitary tracking reference (T_{ref}) around ω_1, with a wider tracking bandwidth in the second design (i.e., $BW_{t2} > BW_{t1}$). This results in a faster reduction of the tracking error (e_t) in the second design for a sudden change of a sinusoidal current reference (i^*) of frequency ω_1. Generally speaking the transient response is, thus, specified and controlled by the designer by means of the bandwith of weight W_t, in a very similar way as is usually done in the design of PR controllers, in this case simpler because of the reduced importance of the phase of the weights.

The controller performance versus energy optimization trade-off is illustrated in Figs. 7-9, where two new designs, identified by subscripts 3 and 4, are considered. Fig. 7 shows the selected admittance (W_y) and control effort (W_u) weights, with the tracking weight (W_t) set to zero. In it, BW_y and BW_u represent the frequency ranges where good controller performance (i.e., good admittance shaping in this case[6]) and energy optimization are the main objectives, respectively. The forth design should result, then, in a bigger admittance shaping bandwidth (BW_{y4}) than the third design (BW_{y3}). This is confirmed in Fig. 8 results, where the admittance of the forth design (Y_4) follows the given reference (Y_{ref}) in a

[5]A good controller performance is considered at frequencies where good admittance or tracking shaping is achieved.

[6]A good admittance shaping is considered to illustrate this trade-off, but similar conclusions could be extracted if good tracking shaping is considered instead as an indication of good controller performance.

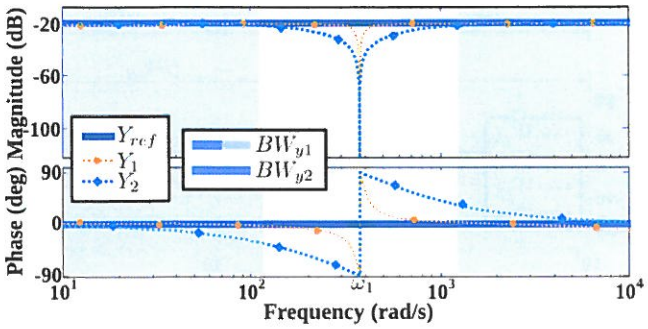

Fig. 5. Admittance versus tracking shaping trade-off example: obtained admittance shaping results.

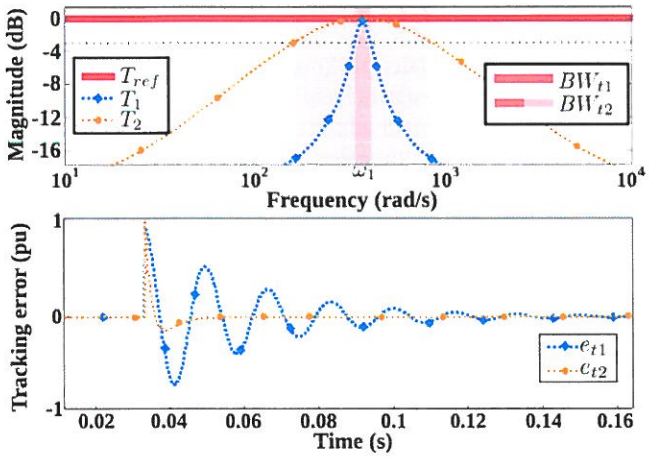

Fig. 6. Admittance versus tracking shaping trade-off example: obtained tracking shaping results (top) and time-domain tracking error (e_t) minimization (bottom). The tracking error is normalized with respect to the current reference (i^*) amplitude.

wider range that the admittance of the third design (Y_3). As Fig. 9 demonstrates, this wider bandwidth induces a higher magnitude of the forth design actuation function ($\bar{\sigma}(\boldsymbol{F}_{u4})$), which means a higher actuation voltage (u) at the system start conditions[7] and, then, in a higher risk of controller saturation.

[7]At the controller initial conditions, the grid voltage v_s is equal to its nominal value and the current reference i^* is set to zero.

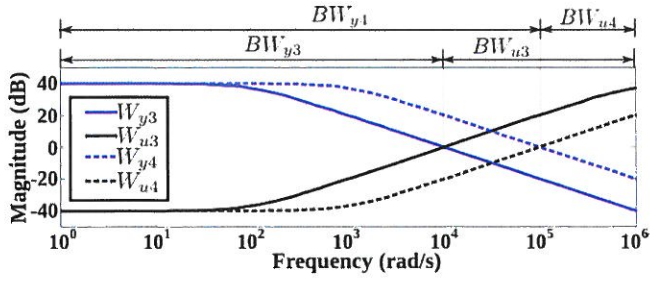

Fig. 7. Admittance shaping versus energy optimization trade-off example: proposed weights selection for both considered designs.

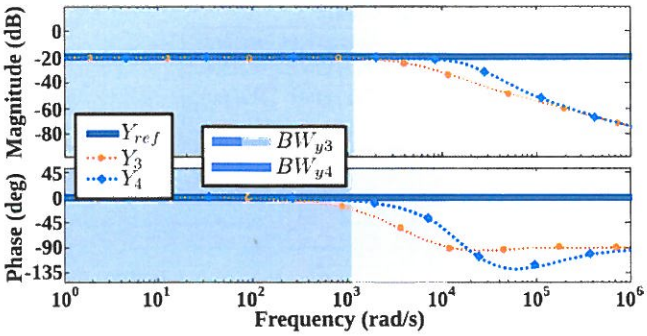

Fig. 8. Admittance shaping versus energy optimization trade-off example: admittance shaping results.

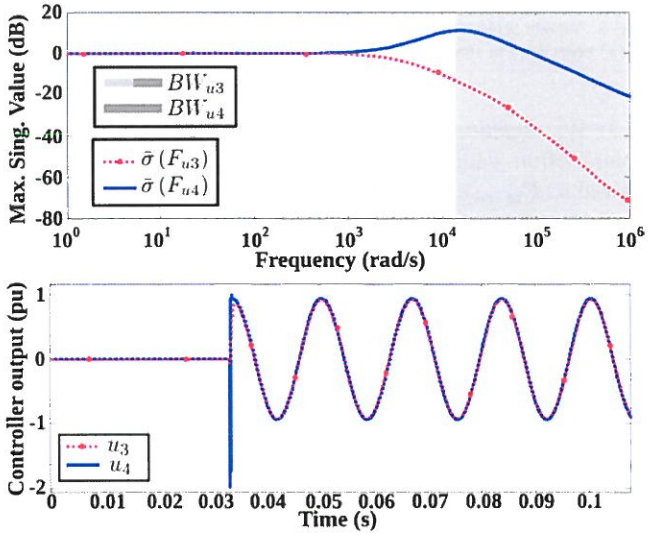

Fig. 9. Admittance shaping versus energy optimization trade-off example: maximum singular values of the actuation function ($\boldsymbol{F}_u$) in the frequency-domain (top) and resulting actuation voltage (u) in the time-domain (bottom). The actuation voltage is normalized to the nominal grid voltage (v_s) amplitude.

D. Design limitations

1) Elements in $\mathbf{P}$ must be linear and proper. Besides, the designed weights should be stable, that is, the use of pure integrators/resonators is not allowed (they are marginally stable). In any case, weights poles/zeros can be placed arbitrarily close to the $j\omega$ axis, so this limitation has a very small effect on the obtained results.

2) The obtained controller $\mathbf{K}$ has the same order than $\mathbf{P}$, so an increase of the design parameters (i.e., weights or model references) order will induce an equal increase of $\mathbf{K}$ order. Order reduction techniques can be used, if necessary, to reduce the computational burden of the synthesized controller.

3) The discrete nature of the implemented controller imposes the presence of one sample delay at the controller output. This induces a bandwidth limitation of approximately $\omega_c = 2\pi f_c < 1/T_s$ rad/s [38] (being T_s the sampling period) that affects both the feedforward and feedback controller terms. This means that admittance shaping can not be obtained

above this frequency, making it impossible to reduce the closed-loop admittance $Y(s)$ below its open-loop value $G_d(s)$ at ω_c.

4) The loop function $L(s) = -GK_i$ relative degree meets the conditions for the application of the Bode sensitivity integral theorem (First Waterbed formula) [38]. It states that an increase in the feedback action of the controller inside a given frequency band comes at the cost of a higher $M_s = \|S(s)\|_\infty$ value and, then, in a reduction of the stability margins. In practice, this means that a wider band of good controller performancefootnote 5 usually results in a less robust system.

E. Controller synthesis. Digital implementation.

The $\mathcal{H}_\infty$ synthesis tools are designed to work with continuous-time plants. The presented controller, however, is executed in a DSP, and thus, a discrete-time controller transfer function is needed. Using a direct discrete-time approximation of a continuous-time controller neglects important dynamics such as the pressence of a PWM modulator, that may be modelled as a zero-order hold, and the presence of a one-sample delay at the plant control input. To include such important elements, the zero-order hold discrete-time equivalent of $G(s)$ is computed and a one-sample delay element z^{-1} is added to it in the z domain. After introducing these dynamic elements in the process, a continuous approximation of this plant is obtained via bilinear transformation, making a frequency prewarping to accurately preserve LCL resonance frequency. The open-loop admittance G_d can be directly included in the augmented plant $\mathbf{P}(s)$ as the grid voltage is, in fact, a continuous disturbance of the process. Frequency weights may also be directly expressed in continuous time, being aware of the aforementioned bandwidth limitations. Once the plant $\mathbf{P}$ is specified, the continuous-time controller, $\mathbf{K}(s)$ is obtained through a regular $\mathcal{H}_\infty$ synthesis process. The final discrete-time controller, $\mathbf{K}(z)$ is then obtained by computing a Bilinear transformation. The use of this procedure, different from the standard ZOH equivalent of the plant, is due to the fact that, although the control system runs in a digital platform, the admittance function of the closed loop plant is a continuous-time function whose input cannot be approximated by a ZOH behaviour.

The snippet displayed on Alg. 1 summarizes the procedure used to synthesize a discrete controller. The open-loop admittance $G_d(s)$ and command-to-output $G(s)$ transfer functions defined in section II-A, along with the selected frequency weights and model-references, form the continuous generalized plant $\mathbf{P}(s)$, whose structure was shown in Fig. 2.

The transfer functions used in $\mathbf{P}$ are created using standard MATLAB library `tf` and `ss` commands. $\mathbf{P}$ is then assembled using the scripting tool `sysic`. Then, the MATLAB Robust Control Toolbox `hinfsyn` command uses the information contained in $\mathbf{P}$ to synthesis a (sub)optimal continuous controller $\mathbf{K}_{cont}(s)$, which is then transformed to its discrete equivalent $\mathbf{K}(z)$ using a bilinear transformation. Continuous to discrete conversions, and vice-versa, are performed using `c2d` and `d2c` commands.

The validity of the controller synthesis process is mainly assessed by means of the obtained γ value. As it was previously mentioned, a large γ value is the result of either too demanding, impossible or conflicting design specifications, and usually results in a poorer minimization of either e_y, e_t or u, even for large $|W_y|$, $|W_t|$ or $|W_u|$ definitions. That is, if a large γ is obtained (typically $\gamma \geq 1$) the designer should redefine the weights and/or the model references dynamics to reduce it until the obtained controller meets the desired performance specifications.

Algorithm 1 Controller synthesis procedure

```
procedure CONTROLLER SYNTHESIS(G,GD,TS)
Weights and model references definition:
    Wu=tf(...); Wt=tf(...); Wy=tf(...);
    Yref=tf(...); Tref=tf(1);
Process model:
    G_ZOH=c2d(G,Ts,'zoh');
    delay=tf([1],[1 0],Ts);
    G_z=delay*G_ZOH;
    G= d2c(G_z,'bilin',...);
P assembly:
    systemnames='G Gd Yref Wy Tref Wt
Wu';
    inputvar ='[vs;i_ref;u]';
    outputvar = '[Wy;Wt;Wu;vs;i_ref;G+Gd]';
    input_to_Wy='[Yref-G-Gd]';
    input_to_Wt='[Tref-G-Gd]';
    input_to_Wu='[u]';
    input_to_Yref='[vs]';
    input_to_Tref='[i_ref]';
    input_to_G= '[u]';
    input_to_Gd= '[vs]';
    P=sysic;
K synthesis:
    [K_cont,γ]=hinfsyn(P,3,1...);
    if (γ > γmax) then goto Weights and [...] definition
    K=c2d(K_cont,Ts,'bilin',...);
    end
```

IV. PROPOSED DESIGNS

This section applies the presented admittance shaping technique to fulfil the objectives exposed in section II-C by means of two different low admittance references Y_{ref}: the first one considers a broad-band low admittance resistive design, while the second one considers a higher order admittance reference with lower values (i.e., dips/notches) at the main grid voltage harmonics. Both admittance references are passive, with a low magnitude at the LCL filter resonance frequency.

A. Broad-band resistive model

In this design, $Y_{ref}(s)$ is defined constant (i.e., resistive) and with the lowest possible value. The third limitation exposed in III-D implies that the minimum obtainable resistive admittance reference $Y_{ref}(s)$ is equal to $G_d(s)$ magnitude at f_c, and, to reduce it, either the sampling time T_s must be reduced or the filter inductances must be increased, as both will result in a smaller magnitude of $G_d(s)$ at ω_c (see Fig. 10).

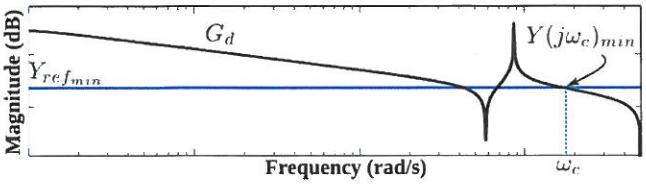

Fig. 10. Minimum obtainable broad-band resistive admittance reference $Y_{ref_{min}}$ as a function of the open-loop admittance G_d and the maximum admittance shaping bandwidth ω_c rad/s.

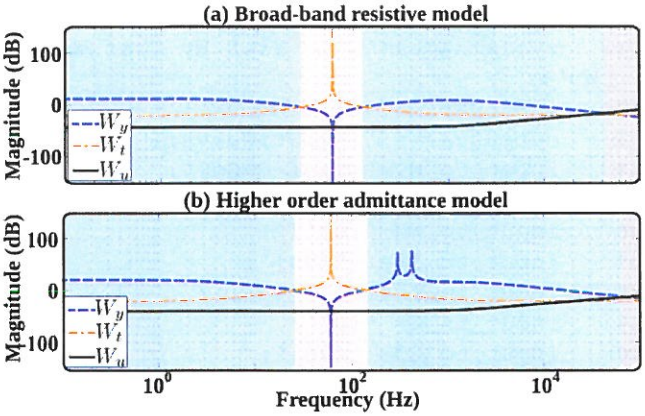

Fig. 11. Frequency domain representation of the selected weights for (a) the broad-band resistive model and (b) the higher order admittance model. Good admittance shaping, tracking shaping and control effort limitation should be obtained in blue, red and black frequency zones, respectively.

Fig. 13(a) shows the representation of the selected resistive admittance $Y_{ref} = 0.06\ \Omega^{-1}$ in the frequency domain, which is the minimum achievable resistive admittance reference for the used filter inductances and sampling frequency (refer to table I).

The next weighting functions are proposed:

$$W_t(s) = K_t \frac{s^2 + 2\zeta_n\omega_1 s + \omega_1^2}{s^2 + 2\zeta_d\omega_1 s + \omega_1^2} \tag{18}$$

$$W_y(s) = K_y \frac{s^2 + 2\zeta_d\omega_1 s + \omega_1^2}{s^2 + 2\zeta_n\omega_1 s + \omega_1^2} \cdot \frac{1}{(1/\omega_y)s + 1} \tag{19}$$

$$W_u(s) = K_u \frac{(1/\omega_{u1})s + 1}{(1/\omega_{u2})s + 1} \tag{20}$$

A frequency domain magnitude representation of them is shown in Fig. 11(a), along with the expected objectives to be fulfilled at each frequency:

1) Admittance shaping zones: A higher admittance weight is defined at both sub- and super-synchronous frequencies thanks to a K_y (19) larger than K_t (18) and K_u (20). This should result in a good admittance shaping at these zones: the higher K_y is, the more minimized the admittance shaping error e_y should be.

2) Tracking zone: At the fundamental (i.e., synchronous) frequency ω_1 a resonant-like gain in W_t (18) and a complementary notch-like gain in W_y (19) should result in a good tracking of the current reference i^* around that frequency. The minimization of the tracking shaping error e_t at ω_1 depends on the defined resonance height, which is equal to the ratio $n_h = \zeta_n/\zeta_d$ in (19) and (18). The higher this ratio is, the smaller the error (i.e., perfect current tracking $i \approx i^*$ can be obtained for very high n_h values). The reference tracking bandwidth can be modified by increasing the K_t value in W_t relative to the K_y value in W_y, or by increasing the ζ_n value in both W_t and W_y to increase the resonance/notch width[8]. The wider this band is, the faster the current reference tracking will be, to the detriment of a reduced admittance shaping range around the fundamental frequency (recall Fig. 5 and Fig. 6).

3) Control stop-band: At high frequencies, the controller actuation stop-band is determined by W_y pole in ω_y (19) and W_u zero in ω_{u1} (20). Decreasing these values should result in a smaller controller bandwidth. A pole at ω_{u2} is added at high frequencies to make W_u proper (see the first limitation in section III-D).

B. Higher order admittance model

The method flexibility allows the definition of more complex admittance models. A superior harmonic attenuation performance is desired in this second design by notching the admittance reference modulus on sensitive frequencies:

$$Y_{ref}(s) = 0.1 \left(\frac{s^2 + 2\zeta_d(5\omega_1)s + (5\omega_1)^2}{s^2 + 2\zeta_n(5\omega_1)s + (5\omega_1)^2} \right) \cdot \ldots \cdot \left(\frac{s^2 + 2\zeta_d(7\omega_1)s + (7\omega_1)^2}{s^2 + 2\zeta_n(7\omega_1)s + (7\omega_1)^2} \right), \tag{21}$$

Y_{ref} in (21) has a resistive behaviour of 0.1 Ω^{-1} at all frequencies except for the fifth ($5\omega_1$) and seventh ($7\omega_1$) harmonic frequencies, where two admittance dips are placed. These dips follows the same formulation than the notch at fundamental frequency in W_y (19); that is, $n_h = \zeta_n/\zeta_d$ will define the dip minimum value and ζ_n the dip bandwidth. In this case, both dips are designed equally, with a minimum gain value $n_h = 10^{-2}$ and enough width to quickly reject the 5^{th} and 7^{th} grid voltage harmonics influence in the controlled current. The selected admittance reference should then result in a current oscillation of 0.1% of the magnitude of eventual 5^{th} and 7^{th} harmonic voltage disturbances ($Y_{ref}(j5\omega_1) = Y_{ref}(j7\omega_1) = 0.001\ \Omega^{-1}$), and an attenuation of 10% for the rest of controlled frequencies ($Y_{ref}(j\omega) = 0.1\ \Omega^{-1}$ for all frequencies except for $5\omega_1$ and $7\omega_1$). The Y_{ref} frequency domain representation for this design is shown in Fig. 13(b). Note that the desired admittance is always inside the passivity-related limits (i.e., $-90 < \angle Y_{ref} < 90$) to increase its stability robustness towards weak grids.

Good admittance shaping is desired again at sub and super synchronous frequencies (including the LCL filter resonance), with a good tracking at the fundamental frequency (ω_1) and higher control effort limitation at high frequencies. Tracking (W_t) and control effort (W_u) weights dynamics are equal to the ones presented in (18) and (20), with a necessary modification in the admittance weight (W_y):

$$W_y(s) = K_y N_{\omega_1}(s) R_{5\omega_1}(s) R_{7\omega_1}(s) \frac{1}{(1/\omega_y)s + 1}, \tag{22}$$

[8]In order to preserve the ratio n_h, ζ_d must increase the same as ζ_n.

TABLE I
EXPERIMENTAL SETUPS PARAMETERS

V_{gN}	120 V	ω_1	$2\pi 60$ rad/s
S_n	2.6‖17.5 kVA	C_{DC}	600‖4700 μF
V^*_{DC}	650 V	C	15‖18 μF
L_1	5.2‖3.4 mH	L_2	4‖1.7 mH
R_1	28.8 mΩ	R_2	18.6 mΩ
T_s	100 μs	T_{sw}	100‖200 μs

where

$$N_{\omega_1}(s) = \frac{s^2 + 2\zeta_{d1}\omega_1 s + \omega_1^2}{s^2 + 2\zeta_{n1}\omega_1 s + \omega_1^2} \quad (23)$$

$$R_{5\omega_1}(s) = \frac{s^2 + 2\zeta_{n5}(5\omega_1)s + (5\omega_1)^2}{s^2 + 2\zeta_{d5}(5\omega_1)s + (5\omega_1)^2} \quad (24)$$

$$R_{7\omega_1}(s) = \frac{s^2 + 2\zeta_{n7}(7\omega_1)s + (7\omega_1)^2}{s^2 + 2\zeta_{d7}(7\omega_1)s + (7\omega_1)^2} \quad (25)$$

The main difference between this new admittance weight and the one used in (19) is the two resonant-like gain increments at the 5^{th} ($R_{5\omega_1}(s)$) and 7^{th} ($R_{7\omega_1}(s)$) harmonic frequencies, introduced to reduce more the admittance shaping error e_y at those frequencies. Fig. 11(b) shows the frequency domain representation of the selected weights for this design.

V. RESULTS

Two experimental platforms, following the single-phase diagram shown in Fig. 1, are implemented to test the two designs defined in section IV. The controller synthesized from the specification defined in section IV-A is implemented in a DS1007 dSPACE system. An AC programmable power supply Chroma 61845 is used to emulate the grid, connected to a 2.6 kVA two-level *Danfoss* VSC with an LCL filter. On the other hand, the controller derived in section IV-B is programmed in C-code and implemented on a Texas Instruments DSP TMS320DSK6713 based control platform. The experimental platform for this controller consists of the connection, through another LCL filter, between an AC programmable power supply Pacific SmartSource 345-AMX, emulating the grid, and a 17.5 kVA two-level *Semikron* VSC.

Table I shows the main parameters considered for each experimental set up, where, if two parameter values are listed, the left and right ones correspond to the *Danfoss* and *Semikron* setups, respectively. S_n, V_{gN} and ω_1 are the nominal power, grid voltage and grid frequency, respectively. V^*_{DC} and C_{DC} are the DC-bus reference voltage and capacitor value. Finally, T_s is the sampling period of the digital controller and T_{sw} is the switching period of the corresponding VSC. It is important to remark the difference between the two setups filter values, being the inductances L_1 and L_2 of the broad-band design bigger to achieve smaller admittance references Y_{ref}.

A. Frequency domain results

Fig. 12 shows the obtained tracking shaping results, being T_{broad} and T_{notch} the obtained tracking transfer functions for the designs presented in sections IV-A and IV-B, respectively.

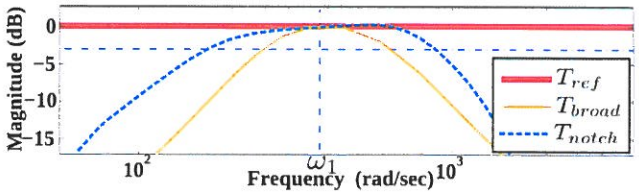

Fig. 12. Tracking shaping results for the two considered designs.

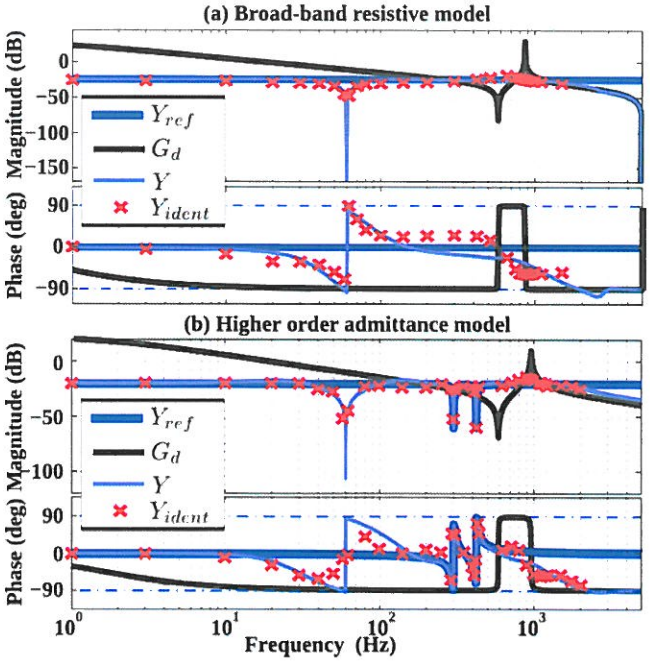

Fig. 13. Obtained input admittance shaping for the two considered designs.

These functions are, as expected, equal to the defined tracking reference T_{ref} around the fundamental frequency ω_1, which will result in a good current reference i^* tracking at this frequency.

Fig. 13(a) shows the obtained closed-loop admittance Y, its open-loop value G_d and the given admittance reference Y_{ref} for the design considered in section IV-A. The obtained admittance Y follows the given reference $Y_{ref} = 0.06\ \Omega^{-1}$ in the desired frequencies (i.e., sub and super synchronous). Y_{ident} shows the experimental measurements of the controlled admittance[9]. The results demonstrate that any voltage harmonic/inter-harmonic at the PCC will be attenuated to a current oscillation of, at most, 6 % of the introduced voltage perturbation for this design.

Fig. 13(b) shows the same results, this time for the design considered in section IV-B. As it can be seen, the 5^{th} and 7^{th} voltage harmonics are highly attenuated to a current oscillation of 0.1% of their magnitude.

The achieved experimental results for admittance Y_{ident} also

[9]To obtain them, three phase small controlled voltage signals are added to the nominal grid voltage at different frequencies by means of the AC power supply. The steady-state current response is then measured. Y_{ident} marks the magnitude/phase relation between the introduced voltage and the measured current at each frequency.

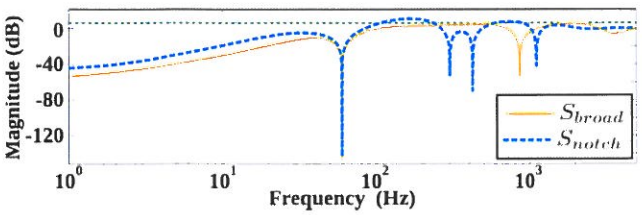

Fig. 14. Sensitivity function magnitude for the two considered designs. The green horizontal dashed line at 6 dB marks the maximum gain value of a system sensitivity function to consider it stand-alone robust.

show that the LCL filter resonance in G_d is well damped in both designs. From a damping point of view, the proposed method has the main advantage of only using the grid current to achieve good results, which means a reduced cost in the number of sensors. Note, in addition, how the theoretical admittance results Y are passive inside the admittance shaping ranges for both designs, with a very small non-passive zone at the fundamental frequency (where good tracking is intended) and at frequencies beyond the controller bandwidth $f_c \approx 1600$ Hz.

B. Robustness results

Fig. 14 shows the magnitude of the sensitivity transfer function $S(s)$ for both considered designs. As it can be seen, its maximum gain value for the broad-band design fulfils the stand-alone stability condition $\|S_{broad}(s)\|_\infty < 6$ dB for stand-alone robustness [38], which is marked in the figure by a green dashed horizontal line. However, the higher order admittance model presents a higher sensitivity peak $\|S_{notch}(s)\|_\infty > 6$ dB induced by the admittance notches at the 5^{th} and 7^{th} harmonics and the water-bed effect [38], and then gives an slightly poorer stand-alone robustness. This is a common concern in current controllers with harmonic rejection capabilities [19].

The presented designs are tested below for two different grid impedance topologies: a purely inductive grid $Z_g(s) = L_g s$ and a resonant inductive-capacitive grid $Z_g(s) = (L_g s)/(L_g C_g s^2 + 1)$. Fig. 19 shows the system closed-loop poles (i.e., roots of $1 + Z_g Y$ in (6)) for changes of L_g[10] in the inductive grid. The system is stable for all inductive grids considered[11]. The same analysis is done in Fig. 20 for changes of $C_g$footnote 10 capacitance in the inductive-capacitive grid, with a L_g fixed to 0.11 pufootnote 10. Some unstable zones can be seen for this case (red lines in Fig. 20) that appear when the resonance of Z_g matches, in frequency, the two non-passive zones of the obtained admittances Y in Fig. 13. The first unstable zone appears in the fundamental frequency ω_1, where the broad-band and the higher order designs interact with the grid for a C_g inside the intervals $[9, 10]$ pu and $[9, 10.77]$ pu, respectively. The second unstable zone appears at high frequencies outside the controller bandwidth f_c, when grids with a C_g inside the intervals $[0.003, 0.025]$ pu and $[0.003, 0.032]$ pu interact with the broad band and the higher order designs, respectively.

Fig. 21 and Fig. 22 show $Y'(s)$ magnitude for some of the previous inductive and inductive-capacitive grid changes, respectively. As it can be seen in Fig. 21, the inductive behaviour of the grid decreases even more the obtained admittances and does not affect the LCL resonance damping. On the other hand, the interaction between the LC resonant grid and the high frequency non-passive zone of both designs generate a Y' resonance in each design: the red boxes in Fig. 22 represent the zones where the system becomes unstable.

As these non-passive zones are not part of the admittance control bandwidth, due to tracking shaping or controller bandwidth limitations (see section III-D), they can only be reduced by a more complex admittance reference that increases system admittance phase (and, then, magnitude) enough prior to their appearance. Some previous works have studied this by including derivative terms in their current controllers [17], [46]. However, this phase increase will provoke bigger actuations and, if feedback is involved, smaller stand-alone margins. In any case, the results in Fig. 22 are taken for the worst case scenario, where the grid resonance is not damped by any resistive element, which is rarely the real case. Additionally, as shown in Fig. 13, experimental results Y_{exp} for both designs present a more resistive behaviour at high frequencies than the theoretical obtained admittances Y, which means that these non-passive zones could even not exist in the real applications.

C. Time-domain results

This subsection presents some time domain experimental results of the obtained grid current controllers for different grid conditions. Fig. 15 shows the tracking results of the broad-band resistive model for a sudden change of the grid current reference i^* with (a) ideal grid conditions and (b) considering an LC resonant grid impedance connected between the LCL filter and the AC power supply. As it can be seen, the current is stable and quickly track the given reference for both cases. Note that, according to the current response in Fig. 15(b), the grid impedance resonance is perfectly damped by the converter resistive admittance. This behaviour is expected according to the admittance magnitude $|Y'(s)|$ value in Fig. 22(a) for the chosen grid impedance parameters (i.e., $L_g = 0.11$ pu and $C_g = 0.05$ pu).

The grid voltage harmonic rejection/attenuation capabilities of the proposed designs are tested as given below. Fig. 16 shows the total harmonic distortion (THD) of the grid current (i) for four different PCC grid voltages (v_s), defined in Table II, and different operational points (i.e., different grid current fundamental values $I(\omega_1)$). As it can be seen, the obtained results for T1 and T2 are much better for the higher order admittance model thanks to its smaller admittance value at the 5^{th} and 7^{th} harmonics. However, this design presents, for the same reason, slightly poorer higher-order harmonics attenuation (see T4 results) than the broad-band resistive design.

[10]Grid impedance parameters are expressed in per unit values of the system nominal impedance $Z_N = 3V_{gN}^2/S_N$ (i.e., $L_N = Z_N/\omega_1$ and $C_N = 1/(Z_N\omega_1)$), considering to that end the nominal power of the *Danfoss* VSC $S_n = 2.6$ kVA.

[11]It is important to remark that some of these grid impedances are not feasible in practice, as their high values will require huge controller actuation for grid current tracking. This analysis only shows the stability robustness of the method.

TABLE II
PCC VOLTAGE HARMONICS FOR THE FOUR CONSIDERED TESTS.

	5^{th}	7^{th}	11^{th}	13^{th}	17^{th}	19^{th}	23^{th}	25^{th}	29^{th}	31^{th}	35^{th}	37^{th}
Test 1 (T1)	0.12 pu	-	-	-	-	-	-	-	-	-	-	-
Test 2 (T2)	0.12 pu	0.1 pu	-	-	-	-	-	-	-	-	-	-
Test 3 (T3)	0.12 pu	0.1 pu	0.07 pu	0.06 pu	-	-	-	-	-	-	-	-
Test 4 (T4)	0.12 pu	0.1 pu	0.07 pu	0.06 pu	0.06 pu	0.06 pu	0.06 pu	0.06 pu	0.05 pu	0.03 pu	0.03 pu	0.03 pu

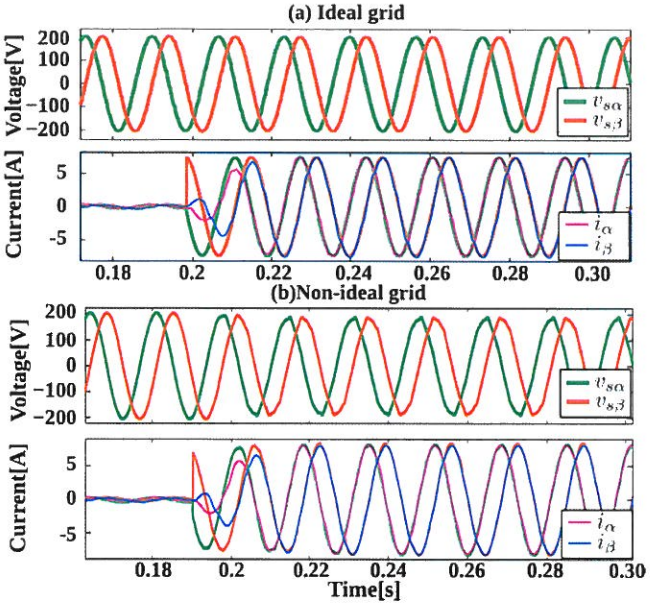

Fig. 15. Time domain experimental tracking results of the broad-band resistive model (a) for an ideal grid impedance ($Z_g = 0$) (b) for a resonant LC-type grid: $L_g = 0.11$ pu and $C_g = 0.05$ pu.

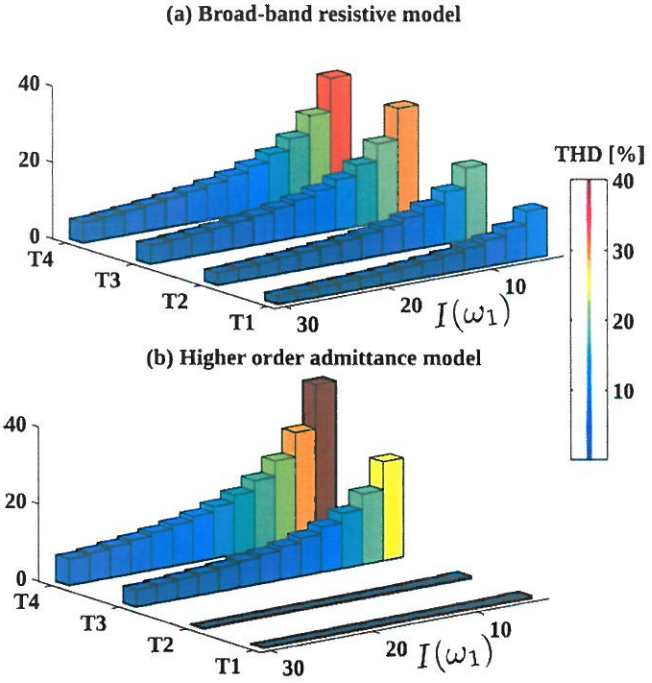

Fig. 16. Obtained THD of the proposed designs for different harmonic test (defined in Table. II).

Fig. 17 and Fig. 18 show further the harmonic rejection/attenuation capabilities of the proposed designs, showing the experimental time domain results to T2 and T4, respectively. As it can be seen, the grid currents i for both designs follow their respective reference i^* after the introduction of grid voltage harmonics in v_s, with reduced current distortion thanks to their low admittance profiles. As expected, the higher order admittance model presents an improved low order harmonic attenuation (see Fig. 17); on the other hand, the broad-band resistive model shows slightly better results for higher-order harmonics (see Fig. 18).

VI. Conclusion

This paper has presented a new design methodology for grid current controllers of grid-connected VSCs based on the system closed-loop admittance shaping. The method gives guarantees in obtaining a controller that simultaneously achieves a low passive admittance and, damp the filter resonances, reject/attenuate the effect of grid voltage disturbances, presents a large robustness towards grid uncertainties and a good current tracking capability, and minimizes converter impact on PCC stability. These objectives are obtained using an intuitive unified design framework that offers convergence and optimality guarantees. Method validity is demonstrated by both simulated and experimental results.

In terms of filter resonance damping, the method needs a reduced number of sensors for its implementation, and exibits good robustness in its damping capabilities in the pressence of grid uncertainty. In terms of harmonics rejection/attenuation, the presented method is able to effectively attenuate a grid voltage disturbances (harmonics and interharmonics) in a wide frequency range, both at sub and super synchronous frequencies, even at frequencies close to the input filter resonance. Moreover, the method is flexible enough to reject the main grid voltage harmonics in a similar way than the classical PR controllers by increasing the order of the defined admittance reference. Finally, as the proposed method can also shape the admittance phase of the controlled system, the presented closed-loop applications are designed to be passive inside their controller bandwidths, making the resulting grid-connected systems very robust to changes of the grid impedance and minimizing the impact of its connection over power system stability.

The underlying $\mathcal{H}_\infty$ synthesis algorithm transfers large part

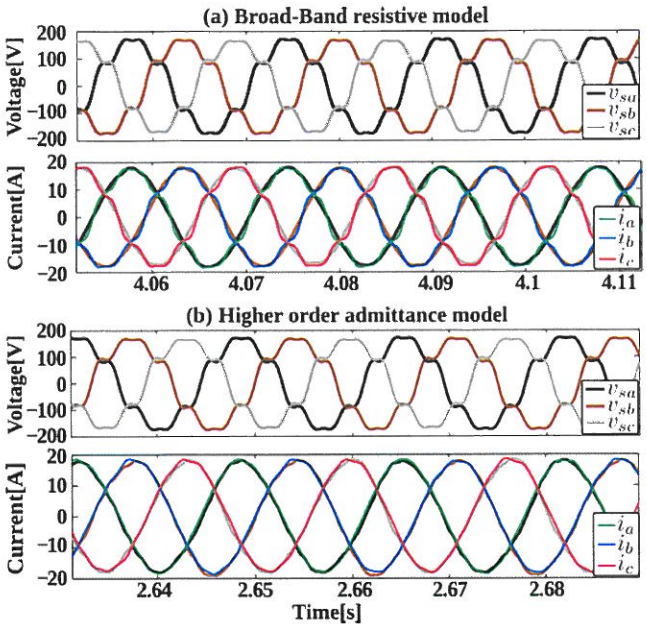

Fig. 17. Experimental time domain results to test 2 (T2) with an ideal grid impedance $Z_g = 0$.

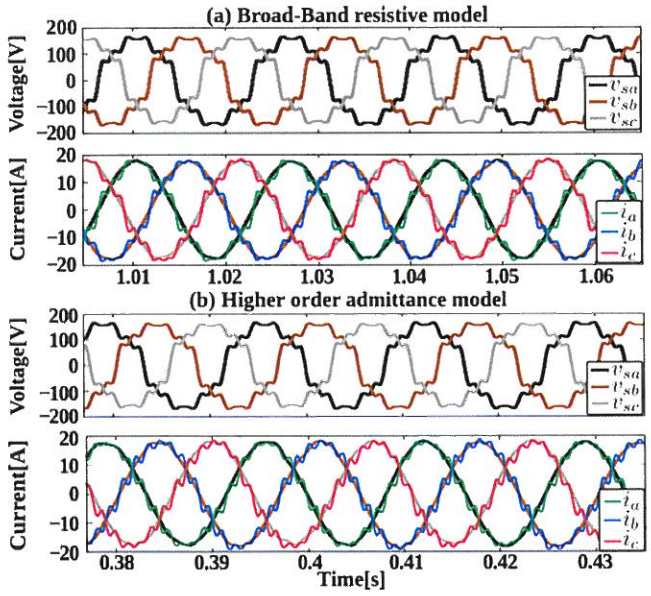

Fig. 18. Experimental time domain results to test 4 (T4) with an ideal grid impedance $Z_g = 0$.

of the controller design complexity to a computational optimization procedure that is controlled using designer-friendly frequencial weights.

The casting of the procedure as a $\mathcal{H}_\infty$ optimization problem also induces conservativeness regarding the trade-off between tracking bandwidth and admittance-shaping bandwidth. Tighter results could be obtained if the algorithm allowed the closed-loop input admittance to vary inside a defined region (possitive-real region) and not track a given resistive reference. Future works may explore this alternative using Kalman-Yakubovich-Popov theorem. On the other hand, the conservativeness induced by a resistive admittance also maximizes system robustness and possitive impact regarding PCC stability, that are very desirable features.

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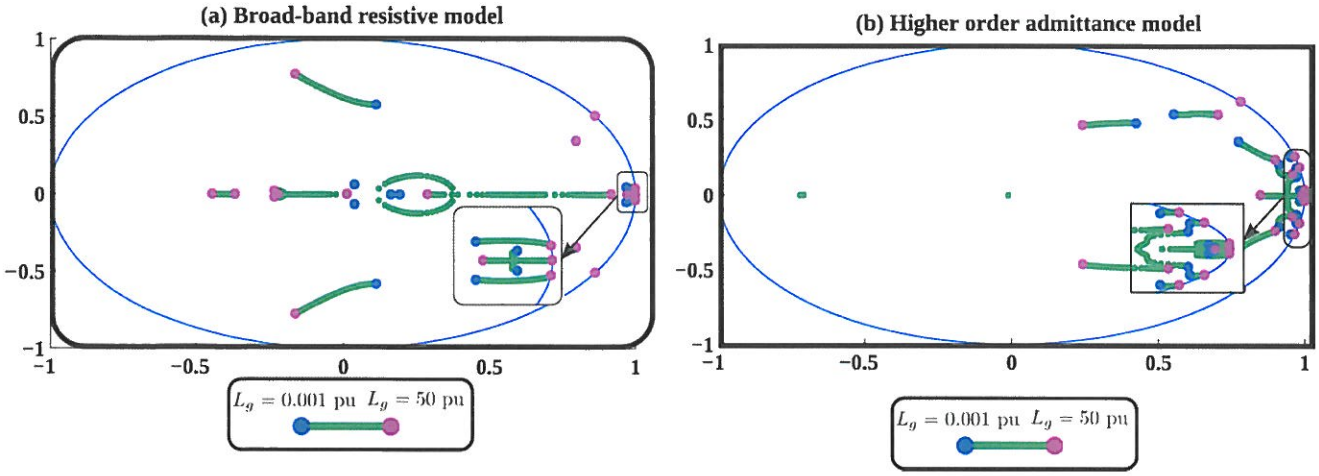

Fig. 19. Closed-loop poles for changes of an inductive grid in both considered designs.

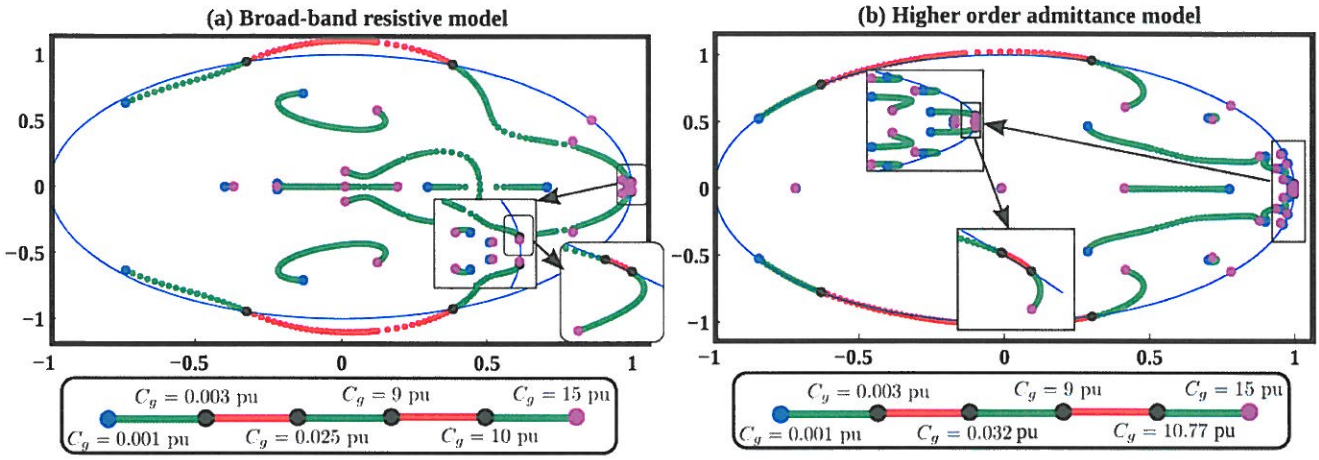

Fig. 20. Closed-loop poles for changes of an inductive-capacitive grid in both considered designs. The red lines represents unstable cases.

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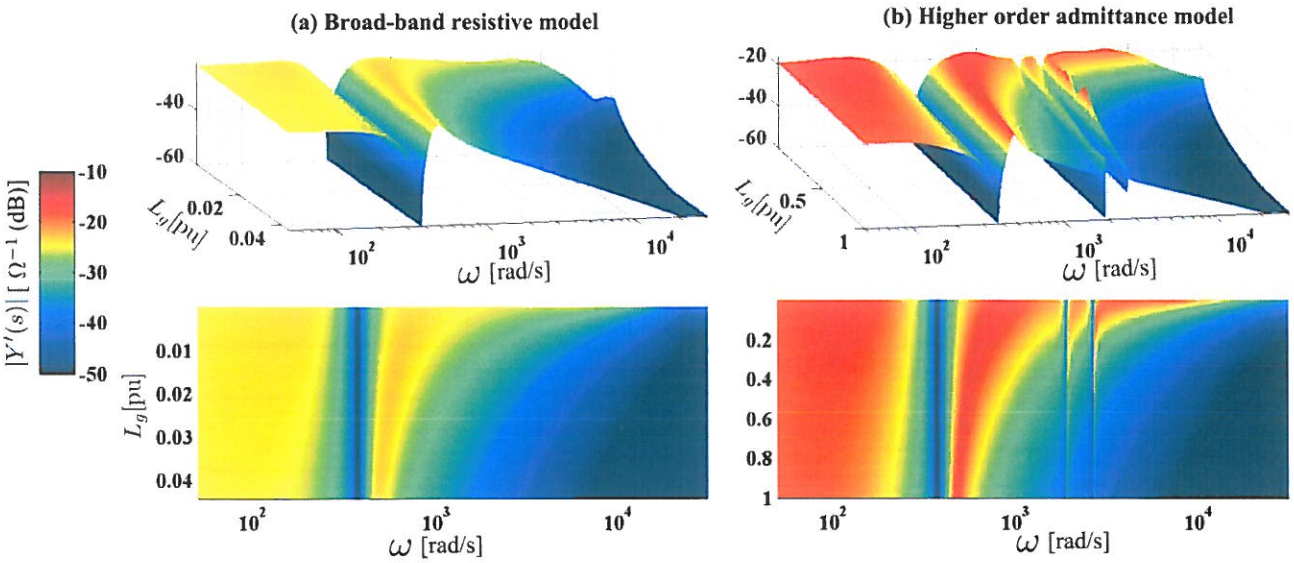

Fig. 21. Admittance magnitude $|Y'(s)|$ for changes of an inductive grid.

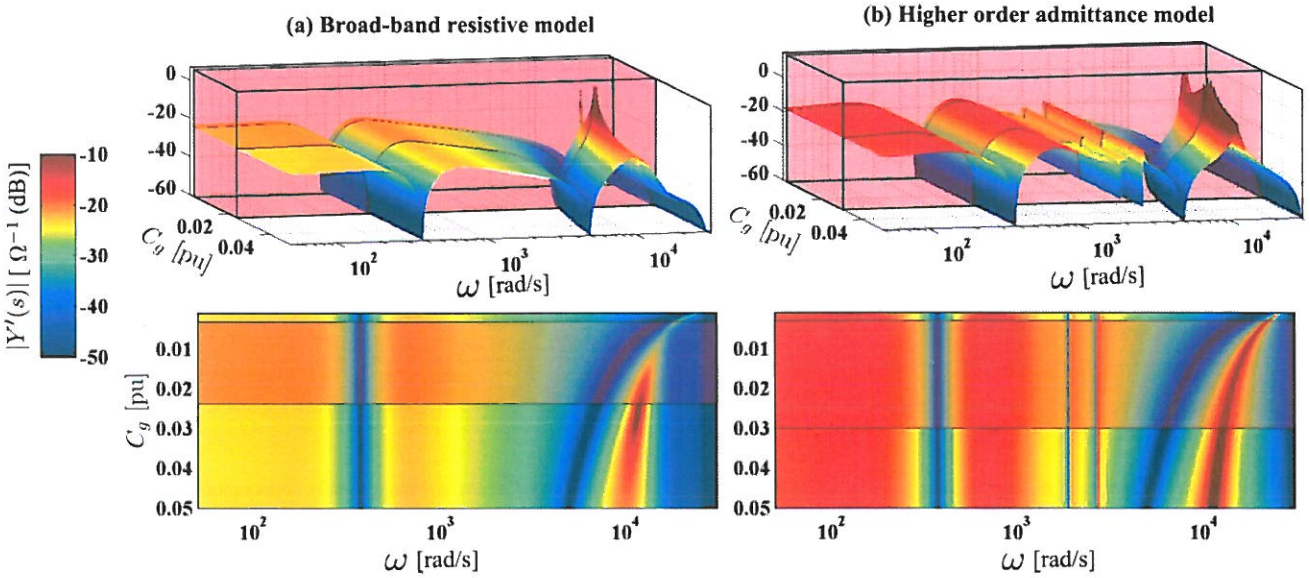

Fig. 22. Admittance magnitude $|Y'(s)|$ for changes of an inductive-capacitive grid. The red box represents C_g interval where the complex system becomes unstable.

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